

**A-SSCC**

IEEE Asian Solid-State Circuits Conference

Second Call for Papers

**IEEE**

IEEE Asian Solid-State Circuits Conference (A-SSCC) 2009

Location: The Grand Hotel, Taipei, Taiwan**Date: November 16, 2009 (Monday) – November 18, 2009 (Wednesday)**

Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

The IEEE A-SSCC 2009 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at the A-SSCC official website <http://a-sscc.org/> around the beginning of April, 2009.

Paper Submission

Prospective authors are invited to submit full-length, four-page manuscripts, including figures, tables and references, to the official A-SSCC 2009 website. All papers will be handled and reviewed electronically. Papers are solicited in the following categories:

Regular Session

- Analog Circuits & Systems:** Amplifiers, comparators, switch capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; display driver circuits; non-linear analog circuits.
- Data Converters:** Nyquist-rate and oversampling A/D and D/A converters, sub-circuits for data converters including sample-and-hold circuits, calibration circuits.
- Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; High-speed low-power digital circuits, power-reduction and management methods for digital VLSI, leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply /substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.
- SoC & Signal Processing Systems:** System-on-chip, microprocessors, network processors, baseband communication processing system & architectures, low-power signal-processing systems; multimedia processors including video, image, audio and voice processing systems; cryptographic- and security-processing circuits and systems; bio-medical/neural signal processors.
- RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits (MMDS, 60GHz); Circuits and sub-circuits for RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.
- Wireline & Mixed-Signal Circuits:** Receivers/transmitters/transceivers for wireline systems including (but not limited to) LAN, WAN, FDDI, Ethernet, token-ring, fiber channel, SONET, SDH, PON, ATM, ISDN, xDSL, cable-modem; optical/electrical data links and backplane transceivers; power-line communication; Clock generation circuits, PLL, DLL, spread-spectrum clock generation.
- Emerging Technologies and Applications:** Advanced circuit technologies and techniques; ultra-low-voltage and sub-threshold logic design; molecular-, organic-, and nano-electronics; flexible substrates and printable electronics; 3D-integration and novel packaging technologies; compound-semiconductor, superconductive, and micro-photonics technologies and circuits; energy sources and energy harvesting; biomedical and ambient-intelligence; emerging wireless applications and circuits; RFID; analog and optical processors, non-transistor-based analog and digital circuits and systems; advanced memory technologies; spintronics; and quantum storage.
- Memory:** Static, dynamic, non-volatile, and read-only memory; magnetic and ferro-electric memory designs and architectures; data storage and multi-bit-cell-based memory designs; embedded memory architectures, cache-memory systems, multi-port memory, and CAM designs, nano-crystal, phase-change, and 3D memories; yield-enhancement redundancy and ECC techniques; and memory testing and built-in self-test.

Special Session

- Industry Program:** This special category accepts only papers based on state-of-the-art products. The paper may cover specifications, applications, state-of-the-art points, chip photos, chip architecture/software, circuits (not necessarily very original, significant improvement is fine), live demo if any, characterization results, and packaging/testing results.
- Student Design Contest:** A student design contest is held among **the accepted papers** with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, SoC, interconnections and statistical design are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Dual submission to other conferences is not allowed. A special issue of the IEEE Journal of Solid-State Circuits will be prepared for publication of the outstanding papers of this conference.

Important dates

June 1, 2009, 20:00 (GMT)

July 28, 2009

September 15, 2009

Paper submission deadline

Acceptance notification

Deadline for final papers submission

Steering Committee **Chair**
 Co-Chair

Conference **Chair**
 Co-Chair
 Organizing Committee Chair

Technical Program Committee **Chair**
 Co-Chair
 Vice-Chair
 Vice-Co-Chair

Chorng-Kuang Wang, National Taiwan University, Taiwan
Takayasu Sakurai, University of Tokyo, Japan
Ming-Kai Tsai, Mediatek Inc., Taiwan
Bing-Lin Gu, Tsinghua U., China
Cheng-Wen Wu, ITRI, Taiwan
Tohru Furuyama, Toshiba Corp., Japan
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Mototsugu Hamada, Toshiba Corp., Japan
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